WHAT IS CLAIMED IS:

1. A semiconductor device having a trench capacitor, wherein

said trench capacitor comprises:

a trench formed in a surface portion of a semiconductor substrate;

an insulating layer formed on the inner wall surfaces of said trench; and

an electrode portion formed inside said trench having said insulating layer, and

said electrode portion has a metal portion.

2. A device according to claim 1, wherein said electrode portion further has a polysilicon portion.

3. A device according to claim 2, wherein said polysilicon portion is formed between said metal portion and said insulating layer on the inner wall surfaces of said trench.

4. A device according to claim 1, wherein said electrode portion further has a metal nitride portion.

5. A device according to claim 4, wherein said metal nitride portion is formed between said polysilicon portion and said metal portion.

6. A device according to claim 1, wherein

the interior of said trench is divided into first, second, and third regions in the order named from the bottom surface along a direction of depth,

said insulating layer is formed on the bottom surface of said trench and on the inner wall surfaces from the bottom surface to the first and second regions of said trench, and

said electrode portion has a structure in which

in the first region, a first polysilicon portion is formed on the bottom surface and inner wall surfaces on which said insulating layer is formed, a first metal nitride portion is formed on the surface of said first polysilicon portion, and a first metal portion is buried in the surface of said first metal nitride portion,

in the second region, a second polysilicon portion is formed on the inner wall surfaces on which said insulating

layer is formed and on the surface of the first region, a second metal nitride portion is formed on the surface of said second polysilicon portion, and a second metal portion is buried in the surface of said second metal nitride portion, and

in the third region, a third polysilicon portion is formed on the inner wall surfaces on which said insulating layer is not formed and on the surface of the second region, a third metal nitride portion is formed on the surface of said third polysilicon portion, a third metal portion is buried in the surface of said third metal nitride portion, and a diffusion region is formed around said third polysilicon portion in said semiconductor substrate.

7. A device according to claim 1, wherein

the interior of said trench is divided into first, second, and third regions in the order named from the bottom surface along a direction of depth,

said insulating layer is formed on the bottom surface of said trench and on the inner wall surfaces from the bottom surface to the first and second regions of said trench, and

said electrode portion has a structure in which

in the first region, a first polysilicon portion is formed on the bottom surface and inner wall surfaces on which said insulating layer is formed, a first metal nitride portion is formed on the surface of said first polysilicon portion, and a first metal portion is buried in the surface of said first metal nitride portion,

in the second region, a second polysilicon portion is formed on the inner wall surfaces on which said insulating layer is formed, a second metal nitride portion is formed on the inner wall surfaces on which said second polysilicon portion is formed and on the surface of the first region, and a second metal portion is buried in the surface of said second metal nitride portion, and

in the third region, a third polysilicon portion is formed on the inner wall surfaces on which said insulating layer is not formed, a third metal nitride portion is formed

on the inner wall surfaces on which said third polysilicon portion is formed and on the surface of the second region, a third metal portion is buried in the surface of said third metal nitride portion, and a diffusion region is formed around said third polysilicon portion in said semiconductor substrate.

8. A device according to claim 1, wherein

the interior of said trench is divided into first, second, and third regions in the order named from the bottom surface along a direction of depth,

said insulating layer is formed on the bottom surface of said trench and on the inner wall surfaces from the bottom surface to the first and second regions of said trench, and

said electrode portion has a structure in which

in the first region, a first metal nitride portion is formed on the bottom surface and inner wall surfaces on which said insulating layer is formed, and a first metal portion is buried in the surface of said first metal nitride portion,

in the second region, a second metal nitride portion is formed on the inner wall surfaces on which said insulating layer is formed and on the surface of the first region, and a second metal portion is buried in the surface of said second metal nitride portion, and

in the third region, a third metal nitride portion is formed on the inner wall surfaces on which said insulating layer is not formed and on the surface of the second region, a third metal portion is buried in the surface of said third metal nitride portion, and a diffusion region is formed around said third polysilicon portion in said semiconductor substrate.

9. A device according to claim 1, wherein said metal contains, as a main component thereof, a metal selected from the group consisting of tungsten (W), tantalum (Ta), nickel (Ni), molybdenum (Mo), titanium (Ti), aluminum (Al), and copper (Cu).

10. A semiconductor device wherein four memory capacitors are arranged into a substantially cross shape around a bit

line contact, and each of said four memory capacitors can be connected to said bit line contact.

11. A semiconductor device comprising:

a bit line contact;

four memory capacitors formed around said bit line contact; and

four gate electrodes formed between said four memory capacitors and said bit line contact,

wherein each of said four memory capacitors and said bit line contact can be connected or disconnected by changing a voltage to be applied to a corresponding one of said four gate electrodes.

12. A device according to claim 11, wherein said memory capacitors are trench capacitors formed in a silicon substrate.

13. A device according to claim 11, wherein

at least two of said four gate electrodes are formed on a predetermined surface, and

the other two of said four gate electrodes are formed below the predetermined surface.

14. A device according to claim 13, wherein

an insulating layer is formed on the side walls of said gate electrodes formed on the predetermined surface, and

said bit line contact is formed in contact with said insulating layer.

15. A semiconductor device comprising:

a bit line contact;

a plurality of gate electrodes formed around said bit line contact; and

a plurality of memory capacitors formed around said bit line contact,

wherein each of said plurality of memory capacitors and said bit line contact can be connected or disconnected by changing a voltage to be applied to a corresponding one of said plurality of gate electrodes, and

at least one of said plurality of gate electrodes is formed on a predetermined surface, and the other of said

plurality of gate electrodes is formed below the predetermined surface.

16. A device according to claim 15, wherein

an insulating layer is formed on the side walls of said gate electrode formed on the predetermined surface, and

said bit line contact is formed in contact with said insulating layer.

17. A device according to claim 15, wherein said memory capacitors are trench capacitors formed in a silicon substrate.

18. A device according to claim 17, wherein said trench capacitors are trench capacitors according to claim 1.

19. A device according to claim 15, wherein said gate electrodes have a metal interconnection layer.

20. A method of fabricating a semiconductor device in which a plurality of trench capacitors are formed around a bit line contact, and each of said plurality of trench capacitors can be connected to or disconnected from said bit line contact, comprising the steps of:

forming said plurality of trench capacitors on a semiconductor substrate;

forming some of a plurality of gate electrodes each for performing switching for a corresponding one of said plurality of trench capacitors, such that said some gate electrodes are buried in the surface of said substrate;

forming the remaining ones of said plurality of gate electrodes on the surface of said substrate so as to be substantially perpendicular to said some gate electrodes;

covering the side surfaces of said remaining gate electrodes with an insulating layer; and

forming said bit line contact in contact with said insulating layer.